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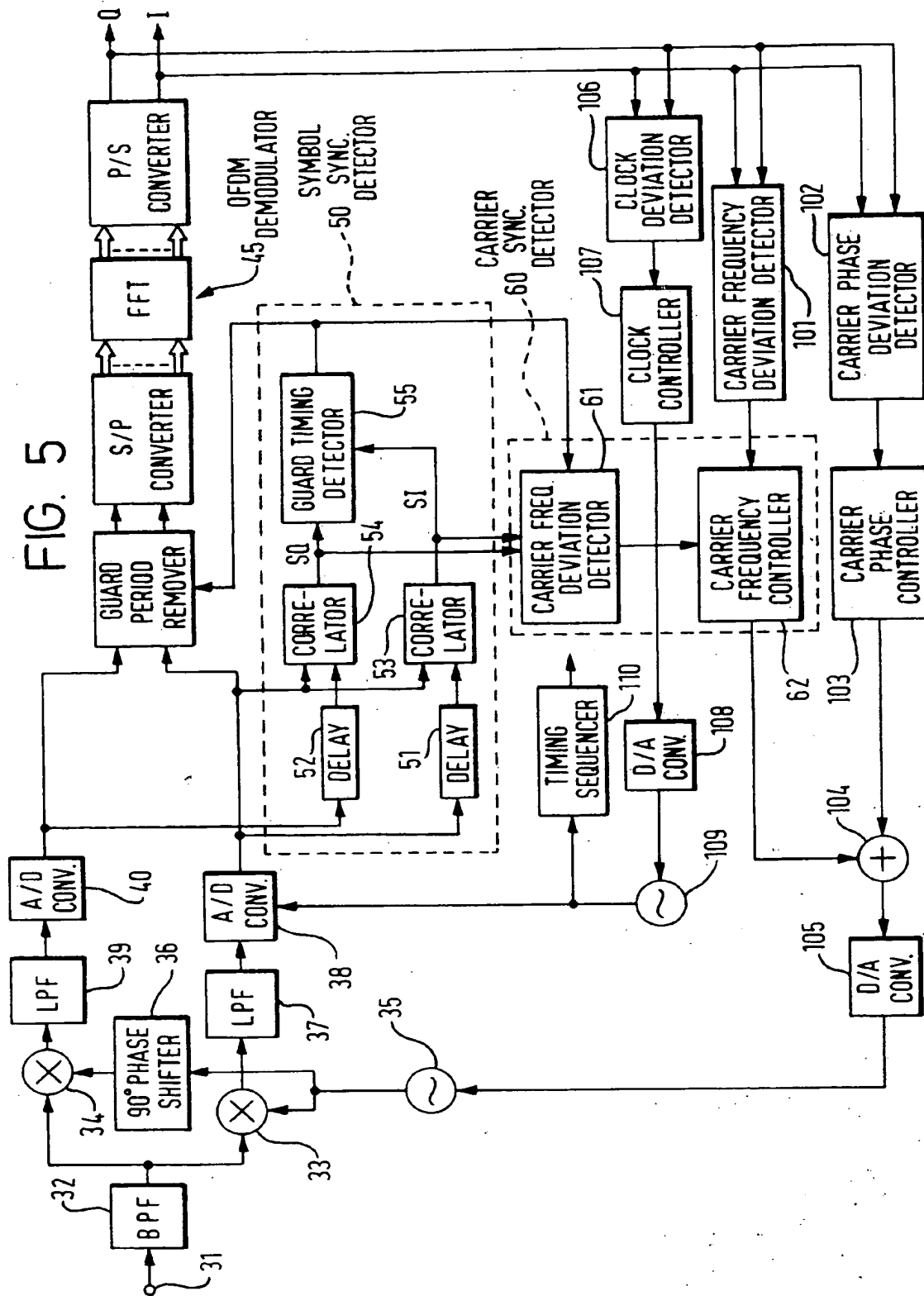
(54) **OFDM Synchronization demodulation circuit.**

(57) The invention provides an OFDM synchronization demodulation circuit which includes a receiving circuit for receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period, an orthogonal axes demodulation circuit for demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the OFDM modulated wave from the receiving circuit, a first delay circuit for delaying the in-phase axis detection signal by the available symbol period, a second delay circuit for delaying the orthogonal axis detection signal by the available symbol period, a correlation calculation circuit for calculating coefficients of the correlations of the in-phase axis detection signal and the orthogonal axis detection signal from the orthogonal demodulation circuit with the output of the first or the second delay circuits, a guard timing detection circuit for detecting a timing of the guard period

in the demodulation outputs from the orthogonal demodulation circuit, and an OFDM signal demodulation circuit for demodulating the OFDM modulated signal by extracting the available symbol period signal only from the demodulated output of the orthogonal demodulation circuit using the timing signal.

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FIG. 5



The present invention relates to an OFDM synchronization demodulation circuit, and more particularly to, an OFDM synchronization demodulation circuit which obtains symbol synchronization and carrier synchronization from information signals.

With the digitization in the broadcasting or mobile radio communication, a digital modulation system has been developed in recent years. In particular, in the mobile radio communication, orthogonal frequency division multiplex (hereinafter referred to as OFDM (orthogonal frequency division multiplex) modulation which is durable against multipass interference has been under the examination for adoption. The OFDM modulation is a system to distribute transmitted digital data in multiple carriers (hereinafter referred to as sub-carriers) which are mutually orthogonal and to modulate each of them. The OFDM has such merits that frequency utilization factor is high and it hardly supplies disturbance to others in addition to a feature that it is hardly subject to the effect of multiple path interference.

FIGURE 1 is a block diagram showing a conventional OFDM modulator/demodulator.

Transmitted data which is input through an input terminal 1 is, for instance, a QPSK modulated or QAM modulated signal. The transmitted data is supplied to a serial/parallel converter 3 of an OFDM modulator 2, where the data is converted into low speed parallel data comprising multiple symbols. The number of symbols per parallel data coincides with the number of sub-carriers. An inverse fast Fourier transform (hereinafter referred to as IFFT) circuit 4 modulates parallel several hundred through several thousand mutually orthogonal sub-carriers by parallel data. The number of sub-carriers is set according to the number of using points of the IFFT circuit 4. The transmitted data which has been OFDM modulated by the IFFT circuit 4 is supplied to a parallel/serial converter 5, where it is converted into serial data and supplied to a guard period adding circuit 6. The guard period adding circuit 6 adds a guard period to the serial data in order to prevent the multiple path interference and outputs the data to a transmission line (not shown).

FIGURE 2 is a typical waveform diagram showing the transmitted data added with a guard period.

As the transmitted data is modulated after distributed into several hundreds or thousands of sub-carriers in the OFDM modulation system, modulation symbol rate of sub-carriers becomes extremely low and the period per one symbol becomes extremely long. Because of the feature, the transmitted data is hardly subject to the effect of a delay time by reflecting waves. Further, the effect of multiple path interference can be removed effectively when a guard period is set in front of the available symbol period. A guard period adding circuit 6 provides a guard period which is a latter half of the available symbol period copied cyclically, as shown in FIGURE 2. If the delay

time of multiple path interference is within the guard period, it is possible to prevent inter-symbol interference by delayed adjacent symbols by demodulating the available symbol period signal only at the time of demodulation.

On the other hand, in the OFDM demodulation circuit 7, data received from a transmission line (not shown) is supplied to a guard period removing circuit 8. The guard period removing circuit 8 extracts signals in the available symbol period from the received data and supplies them to a serial/parallel converter 9. The serial/parallel converter 9 converts serial data into parallel data for every sub-carrier and outputs them to a fast Fourier transform (hereinafter referred to a FFT) circuit 10. The FFT circuit 10 demodulates sub-carriers through the FFT operation. The demodulated signal output from the FFT circuit 10 is converted into serial data by a parallel/serial converter 11 and is output as received data.

By the way, in order that the FFT circuit 10 executes the accurate demodulation, it is necessary to obtain a timing synchronization (hereinafter referred to as the symbol synchronization) of the available symbol period. Further, as transmission data is transmitted after orthogonally modulated, it is also necessary to obtain a carrier synchronization at a receiver section for the proper orthogonal demodulation. As the OFDM modulated wave is a waveform similar to random noise, as shown in FIGURE 2, it is difficult to obtain the symbol synchronization and the carrier synchronization based on the OFDM modulated wave.

So, in a conventional OFDM synchronization demodulation circuit, a reference signal is separately added to attain the symbol synchronization, as described in CCIR Rec. 774. FIGURE 3 is an explanatory diagram for explaining such a conventional symbol synchronizing method.

As described above, a guard period has been added to the transmitted data. That is, as shown in FIGURE 3, transmitted data of one symbol has the available symbol period S and the guard period G. Further, a non-signal period (hereinafter referred to as the null symbol period) for symbol synchronization is added for every several tens of symbol periods. By detecting the null symbol period contained in transmitted data, it is possible to obtain the symbol synchronization at the demodulator section. That is, by detecting a demarcation timing between the null symbol period and the guard period from a modulated wave envelope, the available symbol period timing is obtained based on the detected timing.

FIGURE 4 is a graph for explaining a carrier synchronization method of another conventional OFDM synchronization demodulation circuit, which has been described in "Summary of OFDM Experiments done by the ARTC". In FIGURE 4, frequency is plotted on the X-axis and amplitude of a spectrum plotted on the

Y-axis, and the central frequency band indicates sub-carriers modulated by transmitted data. Sub-carriers at both sides of the frequency band are not modulated and used as pilot carriers 15 and 16. At the demodulator section, the carrier synchronization is attained by detecting the pilot carriers.

However, in a method for executing the symbol synchronization based on null symbols which are cyclically transmitted, null symbols may be disturbed and erroneously detected. So, there was such a problem that the normal demodulating operation was not carried out for a long time until next null symbol was detected in this case. If null symbols are sent frequently to solve the problem, transmission efficiency drops. Further, in a method for executing the carrier synchronization using pilot carriers, the carrier synchronization cannot be attained if pilot carriers are disturbed.

In case of a conventional OFDM synchronization demodulation circuit as described above, there was such a problem that the normal demodulating operation cannot be carried out as no symbol synchronization is attained if a null symbol added to transmitted data is disturbed. In addition, there was also such a problem that no carrier synchronization is attained if pilot carriers are disturbed.

It is, therefore, an object of the present invention to provide an OFDM synchronization demodulation circuit which is capable of executing the symbol synchronization and the carrier synchronization from transmitted information signals only.

In order to achieve the above object, an OFDM synchronization demodulation circuit according to one aspect of the present invention includes a receiving circuit for receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period, an orthogonal axes demodulation circuit for demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the OFDM modulated wave from the receiving circuit, a first delay circuit for delaying the in-phase axis detection signal by the available symbol period, a second delay circuit for delaying the orthogonal axis detection signal by the available symbol period, a correlation calculation circuit for calculating coefficients of the correlations of the in-phase axis detection signal and the orthogonal axis detection signal from the orthogonal demodulation circuit with the output of the first or the second delay circuits, a guard timing detection circuit for detecting a timing of the guard period in the demodulation outputs from the orthogonal demodulation circuit, and an OFDM signal demodulation circuit for demodulating the OFDM modulated signal by extracting the available symbol period signal only from the demodulated output of the ortho-

nal demodulation circuit using the timing signal.

Further, an OFDM synchronization demodulation circuit according to another aspect of the present invention includes a receiving circuit for receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period, an orthogonal axes demodulation circuit for demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the OFDM modulated wave from the receiving means, a first delay circuit for delaying the in-phase axis detection signal by the available symbol period, a second delay circuit for delaying the orthogonal axis detection signal by the available symbol period, a correlation calculation circuit for calculating coefficients of the correlations of the in-phase axis detection signal and the orthogonal axis detection signal from the orthogonal demodulation circuit with the output of the first or the second delay circuit, an OFDM signal demodulation circuit for demodulating the OFDM modulated signal by extracting the available symbol period signal only from the demodulated output of the orthogonal demodulation circuit, a frequency deviation detection circuit for detecting frequency deviation of the orthogonal demodulation circuit based on the correlation coefficient from the correlation calculation circuit, and a detection frequency control circuit for controlling detection frequency of the orthogonal demodulation circuit based on the detection frequency deviation.

In the OFDM synchronization demodulation circuit according to the present invention, as the guard period of the orthogonal frequency division multiplex modulated signal is identical to a part of the available symbol period signal, when delaying amounts of the first and the second delaying means are set based on the available symbol period, the in-phase axis detection signal and the orthogonal axis detection signal from the orthogonal demodulating means are correlative with the outputs of the first and the second delaying means, respectively, if a detected frequency is proper. Further, even when the detected frequency is deviated, the in-phase axis detection signal and the orthogonal axis detection signal are correlative with the outputs of the second and the first delaying means, respectively. In the OFDM synchronization demodulation circuit as claimed in claim 1, the guard timing detection means detects the guard period timing based on the result of correlation and the demodulating means performs the demodulation by extracting the symbol period signal based on the timing signal. In the OFDM synchronization demodulation circuit as claimed in claim 4, the frequency deviation detection means detects a detection frequency deviation of the orthogonal demodulating means based on the result of correlation. The carrier synchronization

is attained by controlling detection frequency using the detection frequency deviation.

Additional objects and advantages of the present invention will be apparent to persons skilled in the art from a study of the following description and the accompanying drawings, which are hereby incorporated in and constitute a part of this specification.

A more complete appreciation of the present invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIGURE 1 is a block diagram showing the OFDM modulator/demodulator;

FIGURE 2 is a waveform diagram showing the OFDM modulated signal;

FIGURE 3 is an explanatory diagram for explaining the symbol synchronization in a conventional example; and

FIGURE 4 is a graph for explaining the carrier synchronization in a conventional example;

FIGURE 5 is a block diagram showing one embodiment of the OFDM synchronization demodulation circuit according to the present invention; FIGURES 6(a) through 6(e) are timing charts for explaining the symbol synchronization detection block shown in FIGURE 5;

FIGURES 7(a) and 7(b) are graphs for explaining the symbol synchronization detection block shown in FIGURE 5;

FIGURES 8(a) and 8(b) are graphs for explaining the symbol synchronization detection block shown in FIGURE 5;

FIGURES 9(a) and 9(b) are graphs for explaining the symbol synchronization detection block shown in FIGURE 5;

FIGURE 10 is a graph for explaining the symbol synchronization detection block shown in FIGURE 5;

FIGURE 11 is a block diagram showing the definite construction of the guard timing detection circuit;

FIGURE 12 is a block diagram showing another example of the guard timing detection circuit;

FIGURE 13 is a block diagram showing the definite construction of the carrier frequency deviation detection circuit shown in FIGURE 5;

FIGURES 14(a), 14(b) and 14(c) are graphs for explaining the carrier synchronization detection block shown in FIGURE 5; and

FIGURE 15 is a block diagram showing another example of the carrier frequency deviation detection circuit.

The present invention will be described in detail with reference to the FIGURES 5 through 15. Throughout the drawings, like or equivalent reference numerals or letters will be used to designate like or

equivalent elements for simplicity of explanation.

Referring now to FIGURE 5, a first embodiment of the OFDM synchronization demodulation circuit according to the present invention will be described in detail. FIGURE 5 is a block diagram showing the embodiment of the OFDM synchronization demodulation circuit.

An OFDM modulated signal which was received by a tuner (not shown) and converted into intermediate frequency band signal (hereinafter referred to as IF signal) is input to an input terminal 31. The OFDM modulated signal input to the input terminal 31 is, for instance, a QAM signal which was OFDM modulated and orthogonal modulated by specific carriers at a transmitter section and then transmitted. Further, the QAM signal is capable of expressing symbols by an I-data corresponding to the real part of a complex form signal and a Q-data corresponding to the imaginary part of the complex form signal. The transmitted OFDM modulated signal does not have the null symbol period, as shown in FIGURE 3, and also it does not have the pilot carrier, as shown in FIGURE 4. The IF signal is supplied to a band-pass filter (hereinafter referred to as BPF) 32, which in turn removes noise outside the passing band and outputs the IF signal to multipliers 33, 34.

Oscillation output frequency (restored carrier) of a local oscillator 35 is controlled by a control signal from a D/A converter 105 which will be described later and is output to the multiplier 33 and also, to the multiplier 34 via a phase shifter 36. The phase shifter 36 obtains Q-axis local oscillation output by shifting the local oscillation output (I-axis local oscillation output) by 90°. The multipliers 33 and 34 perform the orthogonal detection by multiplying the I-axis or Q-axis local oscillation output by the IF signal. The in-phase axis detection output (I-signal) from the multiplier 33 is applied to an A/D converter 38 via a low-pass filter (hereinafter referred to as LPF) 37. Further, the orthogonal axis detection output (Q-signal) from the multiplier 34 is applied to an A/D converter 40 via an LPF 39. These LPFs 37, 39 remove harmonic components of the I-signal or Q-signal, respectively. The A/D converters 38, 40 are supplied with operational clocks from a local oscillator 109, which will be described later, and converting input signal into digital signal, output it to a guard period removing circuit 41 comprising an OFDM demodulator section 45.

The OFDM demodulator section 45 has a similar structure as an OFDM demodulator 7, as shown in FIGURE 1, and is comprised of a guard period removing circuit 41, a serial/parallel conversion circuit 42, an FFT circuit 43 and a parallel/serial conversion circuit 44. The guard period removing circuit 41 is supplied with a guard timing signal from a guard timing detection circuit 55, which will be described later, removing the guard period of OFDM modulated signals (I-signal, Q-signal) and extracting an available symbol per-

mod signal, outputs the OFDM modulated signal to the serial/parallel conversion circuit 42. The serial/parallel conversion circuit 42 converts serial data into parallel data and outputs the parallel data to the FFT circuit 43.

The FFT circuit, regarding the I-signal and the Q-signal as the real part and the imaginary part of the complex form signal, respectively, performs the FFT process. By the FFT process, the synchronization demodulation of each sub-carrier is executed. That is, the real part and the imaginary part of the complex form signal output which has been FFT processed by the FFT circuit 43 become the I-data and the Q-data which are demodulated symbols of each sub-carrier, respectively. These I-data and Q-data are supplied to the parallel/serial conversion circuit 44, which in turn outputs these data after converting them into serial data.

In the present invention, the outputs of the A/D converters 38, 40 are also supplied to a symbol synchronization detection block 50. FIGURES 6(a) through 6(e) are timing charts for explaining the symbol synchronization detection block 50, as shown in FIGURE 5. FIGURE 6(a) shows the output of the A/D converter 38. FIGURE 6(b) shows the output of a delay circuit 51. FIGURE 6(c) shows the output of a correlator 53. FIGURE 6(d) shows the guard timing. And FIGURE 6(e) shows the guard removing gate pulse.

The symbol synchronization detection block 50 is comprised of the delay circuits 51, 52, the correlators 53, 54 and the guard timing detection circuit 55. The delay circuits 51, 52 output the I-signal and the Q-signal to the correlators 53, 54 by delaying them by an available symbol period  $t_s$ . the I-signal from the A/D converter 38 is also input to the correlators 53, 54. The correlator 53 obtains a correlation coefficient of the I-signal with the delayed I-signal at a gate width of the guard period and the correlator 54 obtains a correlation coefficient of the I-signal with the delayed Q-signal.

As described above, the OFDM modulated signal is added with the guard periods G1, G2, ... at the leading section of the available symbol periods S1, S2, ... (See FIGURE 6(a)). The guard periods G1, G2, ... are copied terminal periods G1', G2', ... of the available symbol period S1, S2, ... Therefore, if the I-signal from the A/D converter 38 is delayed by the available symbol period, the timings of the guard periods G1, G2, ... coincide with the timings of the terminating periods G1', G2', ... As the guard period signal is a copied terminal end signal, during the period, the I-signal and its delayed signal are highly correlated. During other periods, as the I-signal is a noisy signal, as shown in FIGURE 2, the correlation of the I-signal with its delay signal is small. Therefore, a correlation coefficient from the correlator 53 becomes gradually high from the start timing of the terminating periods G1, G2, ... and reaches the peak at the end timing of

the terminating period.

A correlation coefficient from the correlator 53 is supplied to the guard timing detection circuit 55. The guard timing detection circuit 55 detects the peak timing, as shown in FIGURE 6(c), and outputs the peak timing to the guard period removing circuit 41 as the guard timing signal (FIGURE 6(d)). The guard period removing circuit 41 generates a guard removing gate pulse (FIGURE 6(e)) based on the guard timing signal and removes the guard period based on the gate pulse.

By the way, the correlation coefficient, as shown in FIGURE 6(c), is that at an ideal demodulation when the carrier synchronization has been attained. On the other hand, if no carrier synchronization is attained, the phase of the demodulated output in the orthogonal demodulation rotates and a correlation coefficient may not become high even during the terminating period. FIGURES 7(a), 7(b) through 10 are graphs showing correlation coefficients obtained from the correlators 53, 54 through the simulation with times plotted at the X-axis and normalized correlation coefficient at the Y-axis. FIGURES 7(a), 8(a) and 9(a) show the correlation coefficient SI between the I-signal and its delayed signal, while FIGURES 7(b), 8(b) and 9(b) show the correlation coefficient SQ between the I-signal and the delayed signal of Q-signal.

FIGURES 7(a) and 7(b) show an example in a case where the carrier synchronization is attained, that is, frequency deviation  $\Delta f$  between the local oscillation frequency (restored carrier frequency) from the local oscillator 35 and carrier frequency is zero (0). In this case, the correlation coefficient SI reaches the peak at the end timing of the terminating period G1', G2', ... as shown in FIGURE 7(a). The I-signal and the Q-signal are signals of which phases are deviated by 90° on the complex plane and haven't been correlated with each other and therefore, the correlation coefficient SQ between the I-signal and the delayed signal of the Q-signal becomes a value near zero (0), as shown in FIGURE 7(b).

FIGURES 8(a) and 8(b) show an example in a case where the carrier frequency deviation  $\Delta f$  is  $f_s/8$  ( $f_s$  is a frequency difference between adjacent sub-carriers). In this case, as the phase rotates by 45° in a time  $t_s$ , the phase of signal G' advances by 45° more than signal G. Therefore, the peak value of the correlation coefficient will become smaller than that when the carrier synchronization is attained, as shown in FIGURE 8(a). Further, the correlation is generated between the I-signal and the delayed signal of the Q-signal, and the correlation coefficient SQ drops to a lower level from the terminating period and reaches the negative peak at the end timing of the terminating period, as shown in FIGURE 8(b).

FIGURES 9(a) and 9(b) show an example of a case where a carrier frequency deviation  $\Delta f$  is  $f_s/4$ . In this case, as the phase rotates by 90° at a time  $t_s$ , the

phase of signal G' advances  $90^\circ$  more than signal G. Therefore, the correlation coefficient SI will become a value near zero (0), as shown in FIGURE 9(a), and the efficient of correlation SQ reaches the negative peak at the end timing of the terminating period, as shown in FIGURE 9(b).

As clear from FIGURES 7(a), 7(b) through 9(a), 9(b), the end timing of the terminating period can be seen from the correlation coefficients SI, SQ even when no carrier synchronization was attained. For this reason, the correlator 54 obtains the correlation coefficient SQ of the I-signal with the delayed signal of the Q-signal and outputs it to the guard timing detection circuit 55.

FIGURE 11 is a block diagram showing the definite structure of the guard timing detection circuit 55, as shown in FIGURE 5. In FIGURE 11, the correlation coefficients SI, SQ are supplied to square circuits 81, 82, respectively. The square circuits 81, 82 square the correlation coefficients SI, SQ, respectively and output the results to an adder 83. The adder 83 adds up the outputs of the square circuits 81, 82 and supplies the result to an LPF 84.

FIGURE 10 is graph showing the arithmetic operating result and shows an example of a case where no carrier synchronization was attained. As shown in FIGURE 10, if the correlation coefficients SI, SQ are squared and added, the added result will reach a peak value at the end timing of the terminating period without depending on a frequency deviation  $\Delta f$ . The LPF 84 smoothes the output of the adder 83 and supplies it to a peak extraction circuit 85. The peak extraction circuit 85 extracts signal in amplitude above a specific level and outputs to a judging circuit 86. The judging circuit 86 detects a peak position from the result of extraction of the peak extraction circuit and outputs a timing signal at the peak position. The timing signal is supplied to a flywheel circuit 87. The flywheel circuit 87 is reset by the timing signal from the judging circuit 86 and outputs a guard timing signal of a fixed cycle based on the timing signal cycle.

FIGURE 12 is a block diagram showing another example of the guard timing detection circuit. In FIGURE 12, the component elements identical to those, as shown in FIGURE 11, are assigned with the same reference numerals and the explanation will be omitted.

In FIGURE 12, absolute value circuits 89, 90 have been adopted instead of the square circuits 81, 82. It is apparent that the peak position is detectable from the result of adding absolute values of the correlation coefficients SI, SQ and the guard timing signal can be obtained even when the guard timing detection circuit 88 in FIGURE 12 [8] is used.

Further, in this embodiment, the correlation coefficients SI, SQ from the correlators 53, 54 are also supplied to a carrier synchronization detection block 60. The carrier synchronization detection block 60 is

comprised of a carrier frequency deviation detection circuit 61 and a carrier frequency control circuit 62.

FIGURE 13 is a block diagram showing the definite structure of the carrier frequency deviation detection circuit, as shown in FIGURE 5. Further, FIGURES 14(a), 14(b) and 14(c) are graphs for explaining the carrier frequency deviation detection circuit, as shown in FIGURE 13. FIGURE 14(a), 14(b) and 14(c) show the relation of the correlation coefficients SI and SQ at the guard timing by plotting carrier frequency deviation  $\Delta f$  at the X-axis and normalized correlation coefficients SI and SQ, respectively or an arc tangent  $SQ/SI$  at the Y-axis.

In FIGURE 13, the correlation coefficients SI and SQ are input to gates 91 and 92 of the carrier frequency deviation detection circuit 61, and the gates 91 and 92 output the correlation coefficients SI and SQ to a calculation unit 93 at the timing of the guard timing signal. The calculation unit 93 obtains an arc tangent of the correlation coefficient  $SQ/SI$  and outputs it to a frequency deviation signal generation circuit 94. The correlation coefficients SI, SQ will change according to the carrier frequency deviation  $\Delta f$  as described above. However, the change in the correlation coefficients SI, SQ at the guard timing has regularity, as shown in FIGURES 14(a) and 14(b), and becomes a function of the carrier frequency deviation  $\Delta f$ . And if the calculation unit 93 obtains an arc tangent of the correlation coefficient  $SQ/SI$ , cross signals at the carrier frequency deviation  $\Delta f = \pm fs, \pm 2fs, \dots$  are obtained, as shown in FIGURE 14(c). The frequency deviation signal generating circuit 94 uses a signal, as shown in FIGURE 14(c), as the carrier frequency deviation signal in order to control carrier frequency. Thus, it becomes possible to pull in carrier frequency to such a level that the carrier frequency deviation  $\Delta f$  becomes integer multiple. The carrier frequency deviation signal is supplied to a carrier frequency control circuit 62.

FIGURE 15 is a block diagram showing another example of the carrier frequency deviation detection circuit.

The correlation coefficient SQ is input to a gate 98 of a carrier frequency deviation detection circuit 97. The gate 98 outputs the correlation coefficient SQ to a frequency deviation signal generation circuit 99 at the timing of guard timing signal. As shown in FIGURE 14(b), the correlation coefficient SQ at the guard timing will become zero (0) if the carrier frequency deviation  $\Delta f$  is integer multiple of  $fs$ . Therefore, the same effect, as shown in FIGURE 13, can be obtained when the frequency deviation signal generation circuit 99 uses a signal, as shown in FIGURE 14(b), as a carrier frequency deviation signal.

While a signal for making the carrier frequency deviation  $\Delta f$  to integer multiple of  $fs$  is obtained from the carrier frequency deviation detection circuit 61 as described above, a signal for controlling frequency

deviation in unit of fs is obtained from the output of the parallel/serial conversion circuit 44. The output of the parallel/serial conversion circuit 44 is supplied to a carrier frequency deviation detection circuit 101 and a carrier phase deviation detection circuit 102. The carrier frequency deviation detection circuit 101 detects frequency deviation of restored carrier by analyzing frequency of each sub-carrier power. In general, maximum and minimum frequency sub-carriers out of OFDM modulated signal sub-carriers are made as guard bands and therefore, are not used (zero carrier). The carrier frequency deviation detection circuit 101 detects deviation of restored carriers by obtaining the zero carrier position from the result of power analysis of sub-carriers. For instance, if restored carrier (local oscillation output) frequency is deviated by fs (carrier frequency deviation  $\Delta f = fs$ ), sub-carrier power of minimum frequency becomes extremely small. It is therefore possible to bring restored carrier frequency in coincidence with carrier frequency at unit of fs by detecting frequency deviation at unit of fs by investigating power of sub-carriers at both ends.

The output of the carrier frequency deviation detection circuit 101 is supplied to the carrier frequency control circuit 62. The carrier frequency control circuit 62 generates a control signal for controlling oscillation frequency of the local oscillator 35 from the output of the carrier frequency deviation detection circuit 101 and a carrier frequency deviation signal from the carrier frequency deviation detection circuit 61 and outputs the generated control signal to an adder 104.

The carrier phase deviation detection circuit 102 detects a phase deviation of restored carriers from out of phase sub-carriers and outputs a phase deviation signal to a carrier phase control circuit 103. The carrier phase control circuit 103 generates a control signal for controlling oscillation phase of the local oscillator 35 using the phase deviation signal and outputs the control signal to the adder 104. The adder 104 adds up the output of the carrier frequency control circuit 62 and the output of the carrier phase control circuit 103 and outputs the added result to a D/A converter 105. The D/A converter 105 converts the output of the adder 104 into an analog signal and outputs the analog signal as a control signal for the local oscillator 35. The oscillation frequency of the local oscillator 35 is controlled based on the output of the D/A converter 105 and the carrier synchronization is thus attained.

Further, the output of the parallel/serial conversion circuit 44 is supplied to a clock deviation detection circuit 106. The clock deviation detection circuit 106 detects a clock deviation from a difference of phase deviations among sub-carriers and outputs a clock deviation signal to a clock control circuit 107. The clock control circuit 107 generates a clock control signal based on the clock deviation signal and outputs it to a D/A converter 108. The D/A converter 108

converts the clock control signal into an analog signal and outputs it to a local oscillator 109. The oscillation frequency of the local oscillator 109 is controlled by the output of the D/A converter 108. Thus, the clock synchronization is attained. Further, the oscillation clock of the local oscillator 109 is supplied to a timing circuit 110 which in turn generates various timing signals.

Next, the operation of the embodiment in the structure as described above will be explained.

The OFDM modulated signal transmitted through a transmission line (not shown) is received by a tuner (not shown) and after converted into the IF signal, it is supplied to the BPF 32 via the input terminal 31. The BPF 32 outputs the IF signal to the multipliers 33, 34 after removing noise. The multipliers 33, 34 are supplied with the I-axis restored carriers or the Q-axis restored carriers and orthogonally demodulate them, respectively. The I-signal from the multiplier 33 is supplied to the A/D converter 38 via the LPF 37 and the Q-signal from the multiplier 34 is supplied to the A/D converter 40 via the LPF 39. The A/D converters 38, 40 convert the I-signal and the Q-signal into digital signals using clocks from the local oscillator 109 and outputs them to the guard period removing circuit 41 of the OFDM demodulation block 45.

In this embodiment, the symbol synchronization for removing the guard period is attained from the OFDM modulated signal. That is, the I-signal and the Q-signal from the A/D converters 38, 40 are supplied to the delaying circuits 51, 52, respectively and delayed by the available symbol period. Then, as shown in FIGURES 6(a) and 6(b), the guard periods G1, G2, ... of the delayed signal of the I-signal and the Q-signal coincide with the timings of the terminating periods G1', G2', ... of the I-signal and if the carrier synchronization has been attained, the I-signal and its delayed signal are mutually related to each other during the period. The correlator 53 obtains a correlation coefficient SI between the I-signal and its delayed signal and outputs it to the guard timing detection circuit 55.

Further, even when no carrier synchronization is attained, there is a correlation between the I-signal and its delayed signal or the I-signal and the delayed signal of the Q-signal during the terminating period, as shown in FIGURES 7(a), 7(b) through 9(a), 9(b). The correlator 45 obtains a correlation coefficient SQ between the I-signal and the delayed signal of the Q-signal and outputs it to the guard timing detection circuit 55. The guard timing detection circuit 55 adds up squares of the correlation coefficients SI and SQ, and generating a guard timing signal at the peak position of the added result and outputs it. As shown in FIGURE 10, the peak position is generated at the end timing of each terminating period. The guard period removing circuit 41 removes the guard period using the guard timing signal. Thus, the symbol synchroniza-



tion is attained.

The OFDM modulated signal with the guard period removed and the available symbol period only extracted is supplied to the serial/parallel conversion circuit 42 where it is converted into parallel data. The FFT circuit 43 performs the FFT process of the parallel conversion signals of the I-signal and the Q-signal regarding them as the real part and the imaginary part of the complex form signal, respectively. As a result, the I-data and the Q-data which are demodulated symbols of sub-carriers are output from the FFT circuit 43. These demodulated symbol data are converted into serial data in the parallel/serial converter 44 and output.

The correlation coefficients SI, SQ from the correlators 53, 54 are supplied to the carrier frequency deviation detection circuit 61. The carrier frequency deviation detection circuit 61 takes in the correlation coefficients SI, SQ at the guard timing and obtains an arc tangent of SQ/SI. As shown in FIGURES 14(a), 14(b) and 14(c), the correlation coefficients SI, SQ at the guard timing are functions of the carrier frequency deviation  $\Delta f$  and arc tangents of SQ/SI become signals which 0 cross at the integer multiple position of  $f_s$ . Using the signal, it is possible to control restored carrier frequency so that the carrier frequency deviation  $\Delta f$  becomes integer multiple of  $f_s$ . The carrier frequency deviation detection circuit 61 outputs the signal to the carrier frequency control circuit 62 as a carrier frequency deviation signal.

The carrier frequency control circuit 61 generates a control signal for controlling oscillation frequency of the local oscillator 35 based on the output of the carrier frequency deviation detection circuit 101 and the carrier frequency deviation signal and outputs it to the adder 104. Further, the carrier phase deviation detection circuit 102 detects a phase deviation of restored carrier based on the phase deviation of sub-carrier, and the carrier phase control circuit 103 generates a control signal for controlling the local oscillator 35 based on the phase deviation and supplies it to the adder 104. The output of the carrier frequency control circuit 62 and that of the carrier phase control circuit 103 are added up by the adder 104, converted into an analog signal by the D/A converter 105 and supplied to the local oscillator 35. Thus, the oscillation of the local oscillator 35 is controlled and the carrier synchronization is attained.

Further, the output of the parallel/serial conversion circuit 44 is also supplied to the carrier frequency deviation detection circuit 101 and the carrier phase deviation detection circuit 102. Frequency of sub-carrier power is analyzed by the carrier frequency deviation detection circuit 101 and a signal for controlling restored carrier frequency in unit of  $f_s$  is supplied to the carrier frequency control circuit 62.

The clock synchronization and the carrier synchronization are attained using the output of the par-

allel/serial conversion circuit 44. That is, the output of the parallel/serial conversion circuit 44 is supplied to the clock deviation detection circuit 106 to obtain a clock deviation signal based on a difference of phase deviations of sub-carriers. The clock control circuit 107 generates a clock control signal based on the clock deviation signal and controls oscillation of an imaginary part oscillator 109. The clock synchronization is thus attained.

As described above, in this embodiment the symbol synchronization is attained by obtaining a guard timing from the result of correlation between the orthogonal demodulated output and its delayed signal utilizing the fact that a signal in the guard period is a copied signal of that in the end period of the available symbol period. In addition, from the fact that the relation between the result of correlation of the orthogonal demodulated output with its delayed signal and the carrier frequency deviation changes at the cycle of carrier interval  $f_s$ , restored carrier frequency accurately coincides with carrier frequency by controlling restored carrier frequency based on the result of correlation, and furthermore, by controlling deviation in unit of  $f_s$  based on sub-carrier power of the FFT demodulated output and thus, the symbol synchronization and the carrier synchronization are attained based on information signal only, and it is possible to attain the positive symbol and the carrier synchronizations without using a special reference signal or a pilot carrier and to achieve the OFDM demodulation durable against disturbance.

Further, although the correlation coefficients SI, SQ represent the correlation between the I-signal and its delayed signal and that between the I-signal and the delayed signal of the Q-signal, respectively, in the above embodiment, the correlation between the Q-signal and its delayed signal may be used as the correlation coefficient SI. In addition, the correlation between the Q-signal and the delayed signal of the I-signal may be used as the correlation coefficient SQ. Further, the correlation coefficients SI and SQ can be combined freely as desired.

As described above, the present invention can provide an extremely preferable OFDM synchronization demodulation circuit.

While there have been illustrated and described what are at present considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teaching of the present invention without departing from the central scope thereof. Therefore, it is intended that the present invention not be limited to the particular embodiment disclosed as the best mode contemplated

for carrying out the present invention, but that the present invention includes all embodiments falling within the scope of the appended claims.

The foregoing description and the drawings are regarded by the applicant as including a variety of individually inventive concepts, some of which may lie partially or wholly outside the scope of some or all of the following claims. The fact that the applicant has chosen at the time of filing of the present application to restrict the claimed scope of protection in accordance with the following claims is not to be taken as a disclaimer or alternative inventive concepts that are included in the contents of the application and could be defined by claims differing in scope from the following claims, which different claims may be adopted subsequently during prosecution, for example, for the purposes of a divisional application.

## Claims

### 1. An OFDM synchronization demodulation circuit comprising:

receiving means for receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period;

orthogonal axes demodulation means for demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the OFDM modulated wave from the receiving means;

first delaying means for delaying the in-phase axis detection signal by the available symbol period;

second delaying means for delaying the orthogonal axis detection signal by the available symbol period;

correlation calculation means for calculating coefficients of the correlations of the in-phase axis detection signal and the orthogonal axis detection signal from the orthogonal demodulation means with the output of the first or the second delay means;

guard timing detection means for detecting a timing of the guard period in the demodulation outputs from the orthogonal demodulation means; and

OFDM signal demodulation means for demodulating the OFDM modulated signal by extracting the available symbol period signal only from the demodulated output of the orthogonal demodulating means using the timing signal.

### 2. An OFDM synchronization demodulation circuit as claimed in claim 1, characterized in that the

guard timing detection means detects the timing signal by adding the square of the correlation coefficient of the in-phase axis detection signal with the output of the first delay means or the correlation coefficient of the orthogonal axis detection signal with the output of the second delaying means and the square of the correlation coefficient of the in-phase axis detection signal with the the output of the second delaying means or the correlation coefficient of the orthogonal axis detection signal with the output of the first delaying means.

3. An OFDM synchronization demodulation circuit as claimed in claim 1, characterized in that the guard timing detection means detects a timing signal by calculating an absolute value of the correlation coefficient of the in-phase axis detection signal with the output of the first delaying means or the correlation coefficient of the orthogonal axis detection signal and the output of the second delaying means and an absolute value of the in-phase axis detection signal with the output of the second delaying means or the correlation coefficient of the orthogonal detection axial signal with the output of the first delaying means, and then, by adding up the absolute values.

### 4. An OFDM synchronization demodulation circuit comprising:

receiving means for receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period;

orthogonal axes demodulation means for demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the OFDM modulated wave from the receiving means;

first delaying means for delaying the in-phase axis detection signal by the available symbol period;

second delaying means for delaying the orthogonal axis detection signal by the available symbol period;

correlation calculation means for calculating coefficients of the correlations of the in-phase axis detection signal and the orthogonal axis detection signal from the orthogonal demodulation means with the output of the first or the second delay means;

OFDM signal demodulation means for demodulating the OFDM modulated signal by extracting the available symbol period signal only from the demodulated output of the orthogonal demodulating means;

frequency deviation detection means for detecting frequency deviation of the orthogonal demodulating means based on the correlation coefficient from the correlation calculation means; and

detection frequency control means for controlling detection frequency of the orthogonal demodulating means based on the detection frequency deviation.

5. A method for demodulating an OFDM synchronization, comprising the steps of:

receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period;

demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the received OFDM modulated wave;

delaying the in-phase axis detection signal by the available symbol period;

delaying means for delaying the orthogonal axis detection signal by the available symbol period;

calculating coefficients of the correlations of the demodulated in-phase axis detection signal and the orthogonal axis detection signal;

detecting a timing of the guard period in the demodulated outputs; and

demodulating the OFDM modulated signal by extracting the available symbol period signal only from the demodulated output using the timing signal.

6. A method as claimed in claim 5, wherein the guard timing is detected by adding the square of the correlation coefficient of the in-phase axis detection signal with the output of the first delay means or the correlation coefficient of the orthogonal axis detection signal with the output of the second delaying means and the square of the correlation coefficient of the in-phase axis detection signal with the the output of the second delaying means or the correlation coefficient of the orthogonal axis detection signal with the output of the first delaying means.

7. A method as claimed in claim 5, wherein the guard timing is detected by calculating an absolute value of the correlation coefficient of the in-phase axis detection signal with the output of the first delaying means or the correlation coefficient of the orthogonal axis detection signal and the output of the second delaying means and an absolute value of the in-phase axis detection signal

with the output of the second delaying means or the correlation coefficient of the orthogonal detection axial signal with the output of the first delaying means, and then, by adding up the absolute values.

8. A method for demodulating an OFDM synchronization, comprising the steps of:

receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period;

demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the received OFDM modulated wave;

delaying the in-phase axis detection signal by the available symbol period;

delaying means for delaying the orthogonal axis detection signal by the available symbol period;

calculating coefficients of the correlations of the demodulated in-phase axis detection signal and the orthogonal axis detection signal;

demodulating the OFDM modulated signal by extracting the available symbol period at signal only from the demodulated output;

detecting frequency deviation of the orthogonal demodulating means based on the calculated correlation coefficient;

providing a reference frequency for the OFDM demodulated signal; and

controlling the reference frequency based on the detected frequency deviation.

FIG. 1 (PRIOR ART)

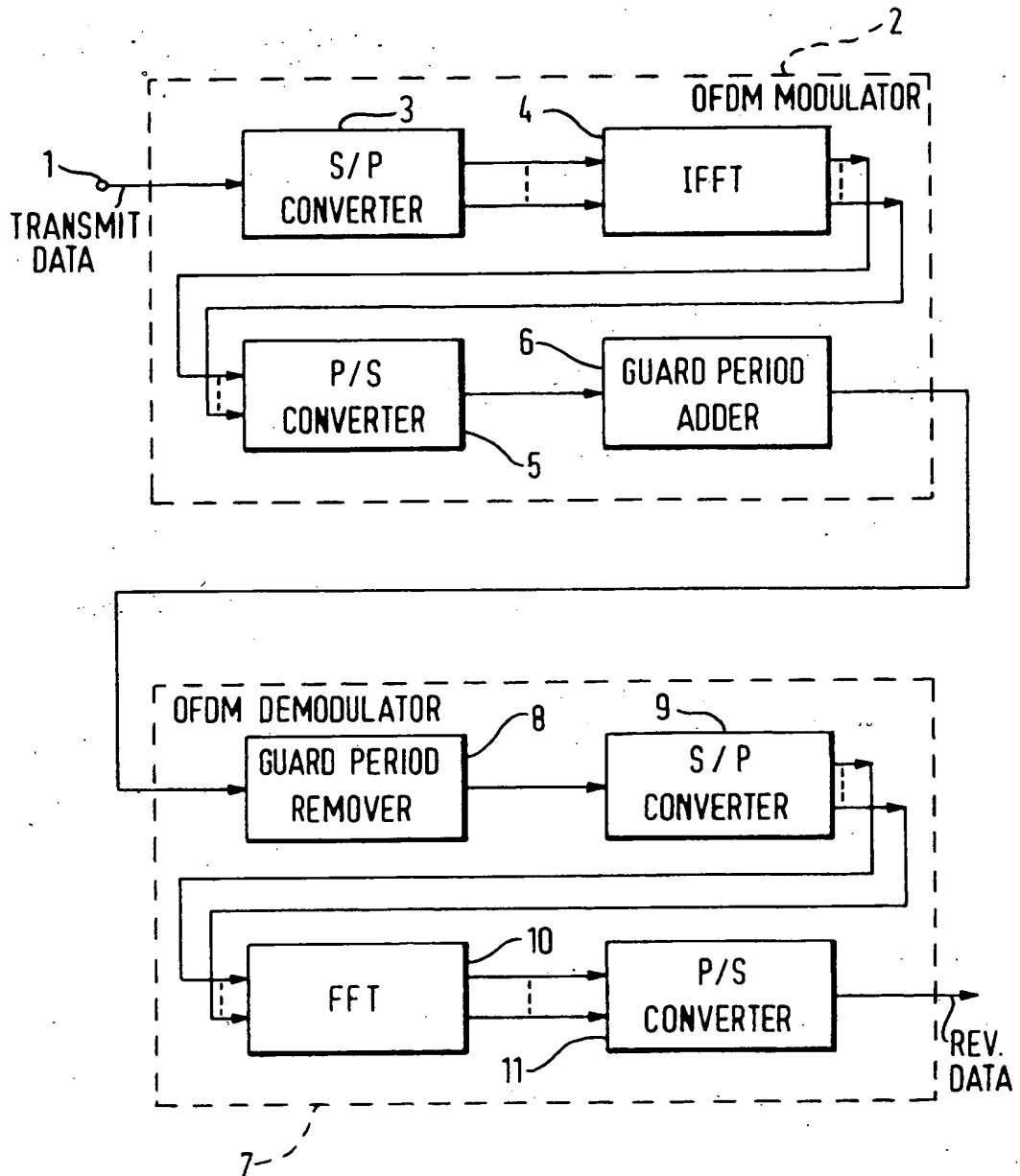


FIG. 2

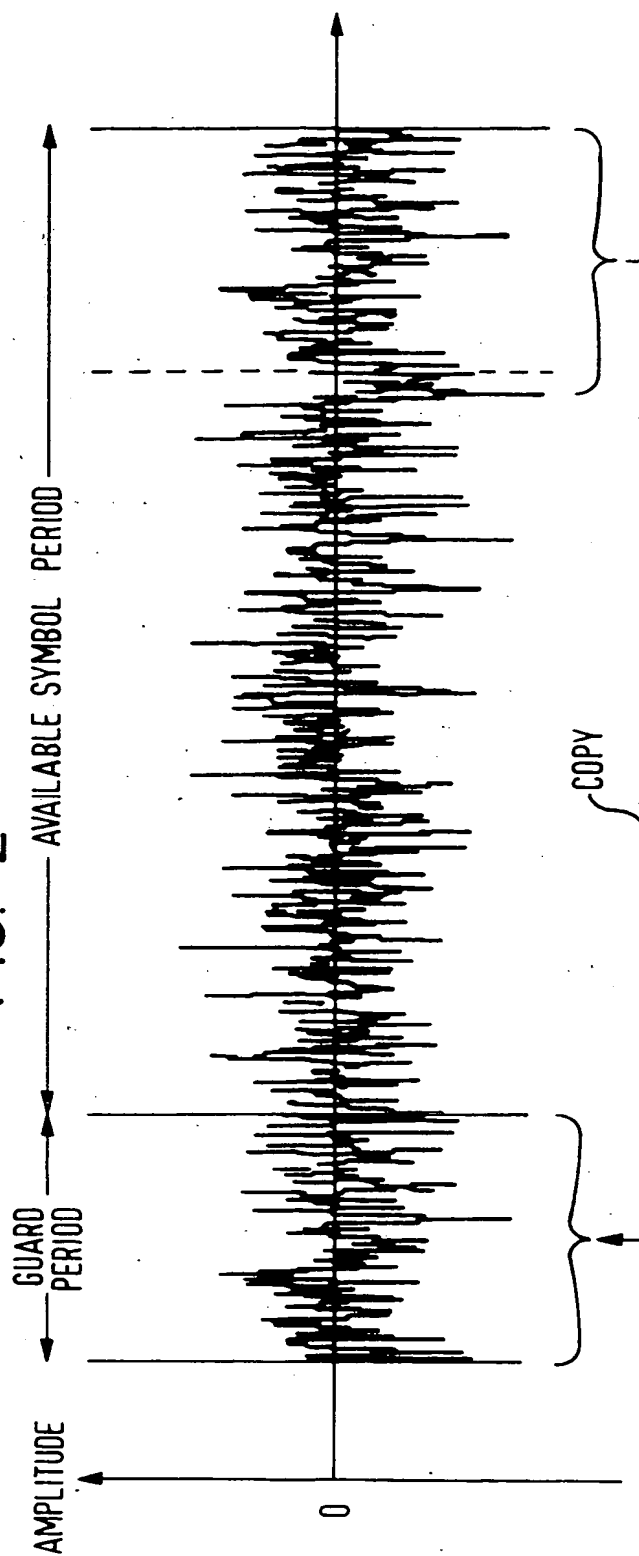


FIG. 3

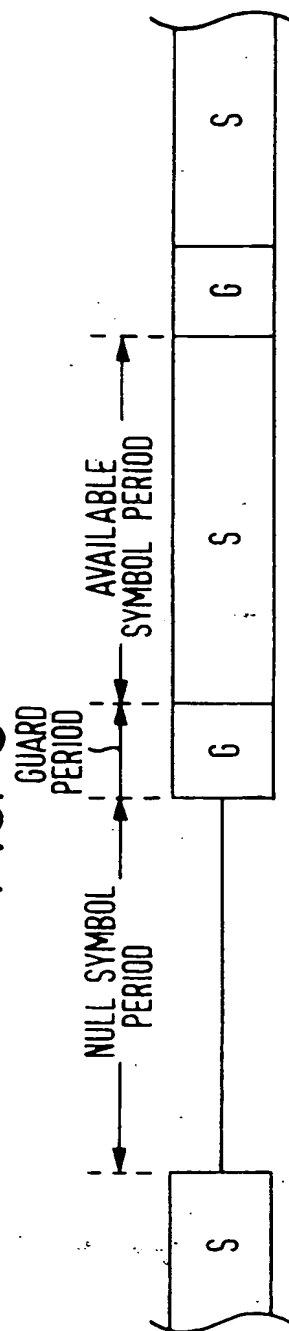


FIG. 4

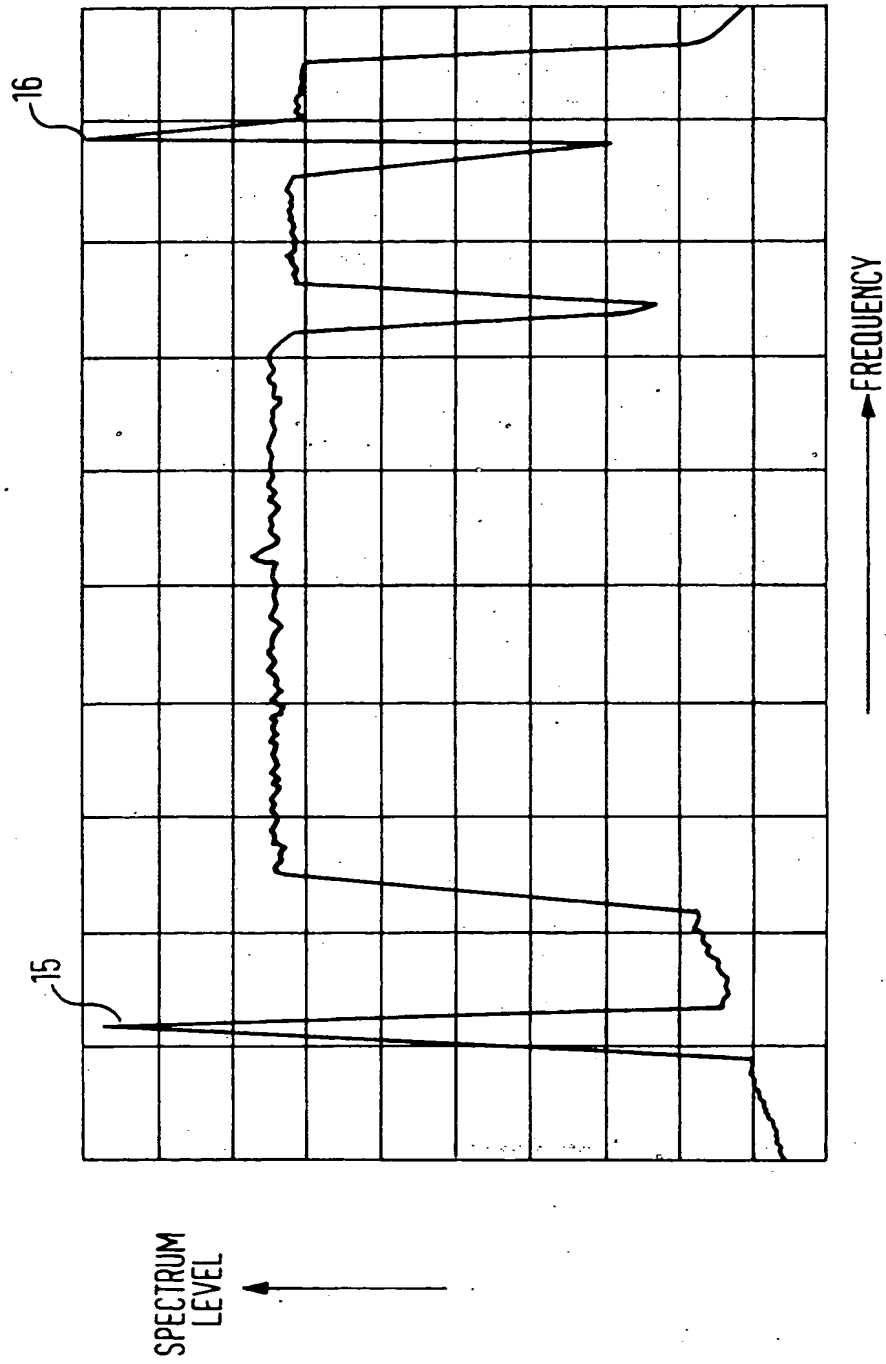


FIG. 5

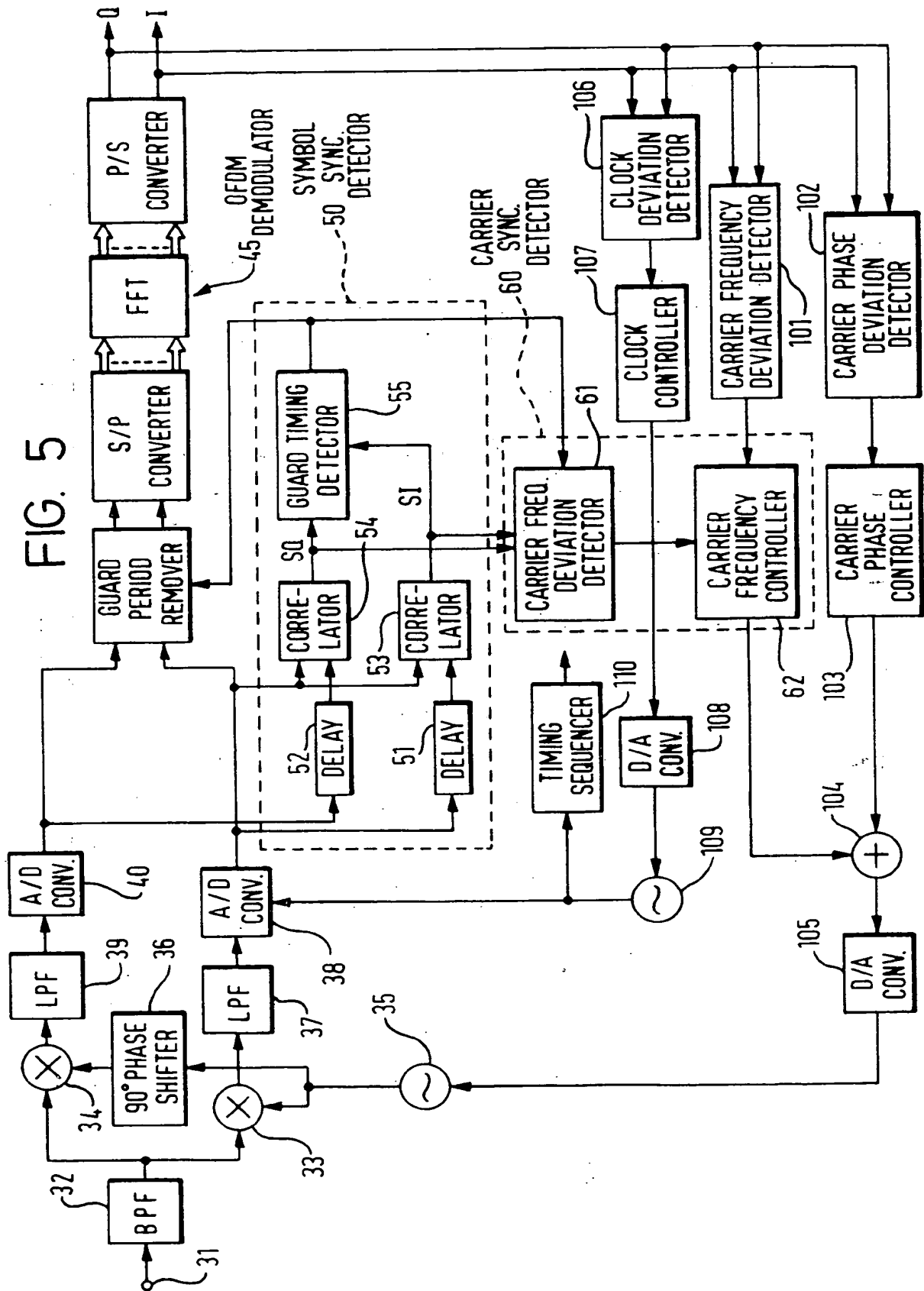


FIG. 6(a)

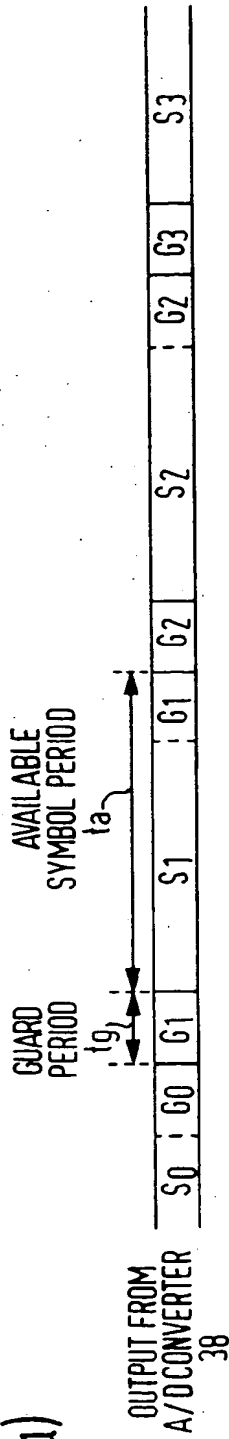


FIG. 6(b)



FIG. 6(c)

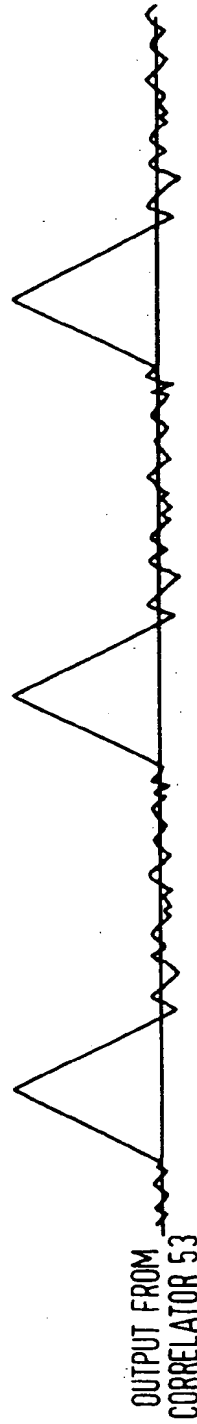


FIG. 6(d)

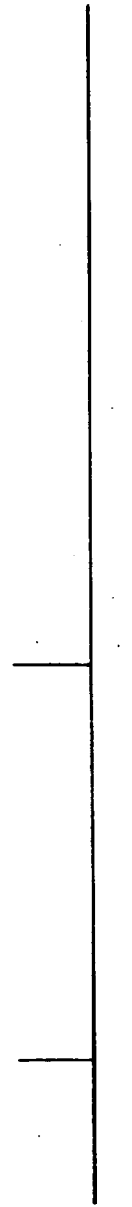


FIG. 6(e)

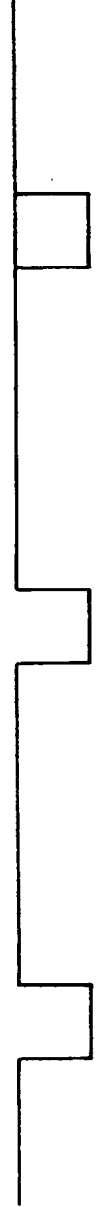




FIG. 7(a)

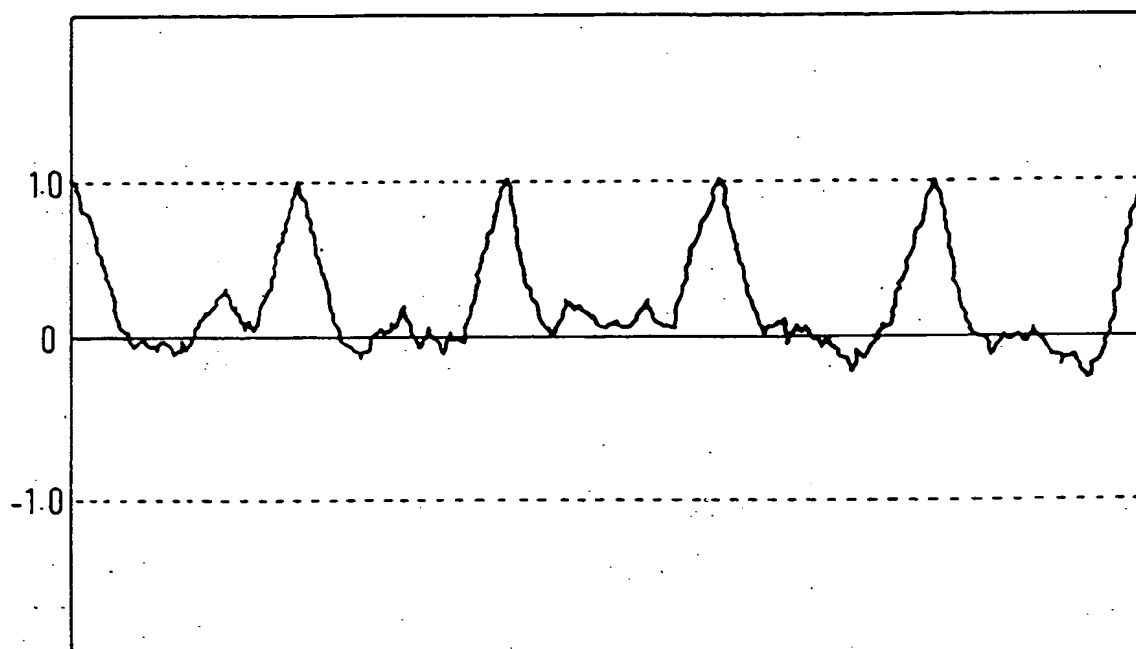


FIG. 7(b)

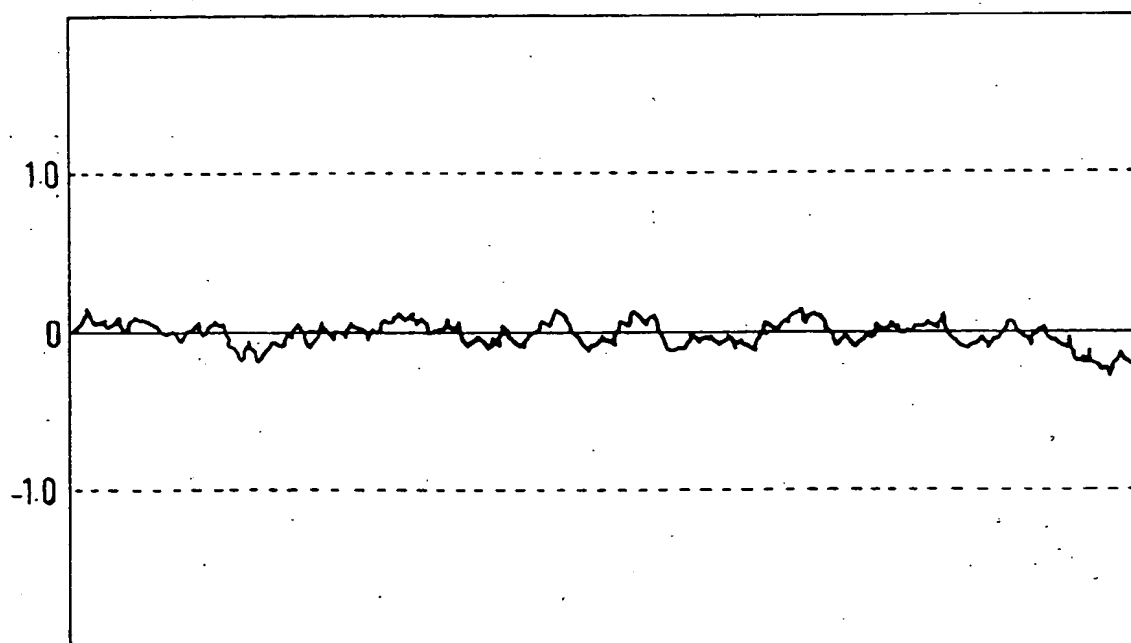


FIG. 8(a)

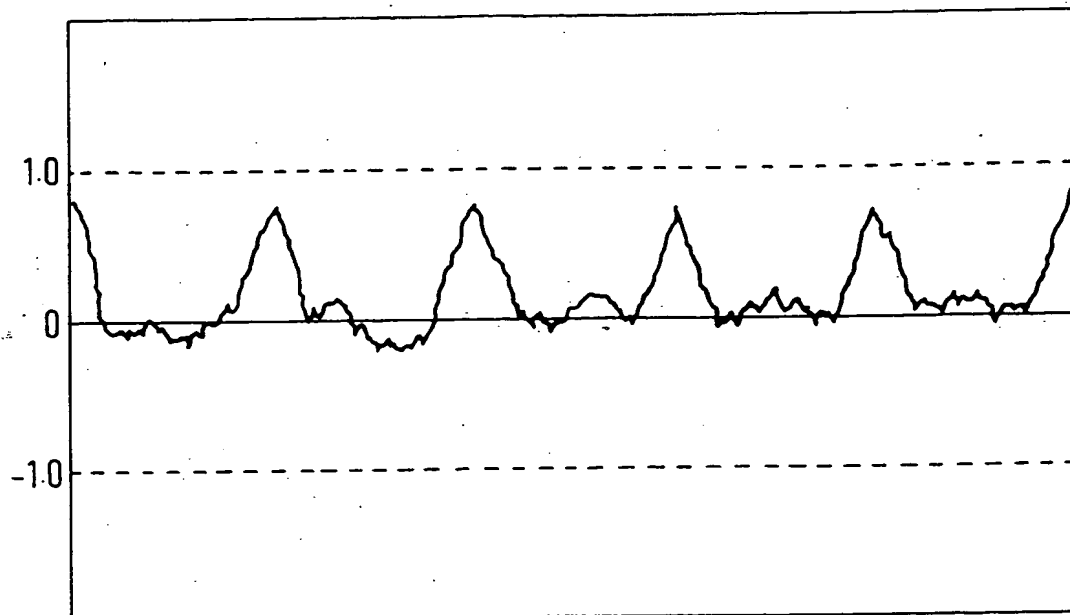


FIG. 8(b)

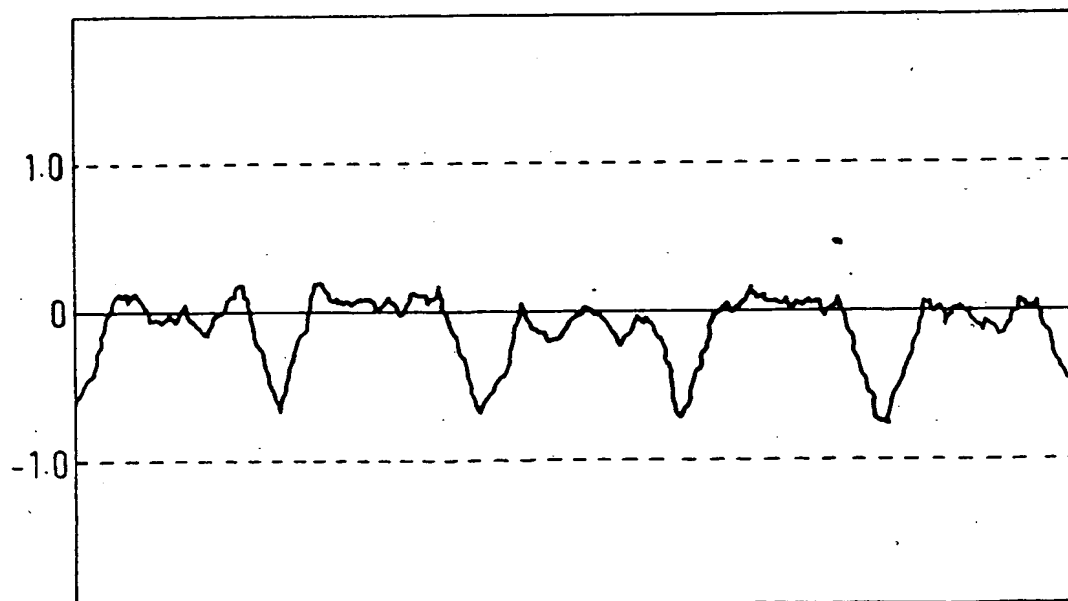


FIG. 9(a)

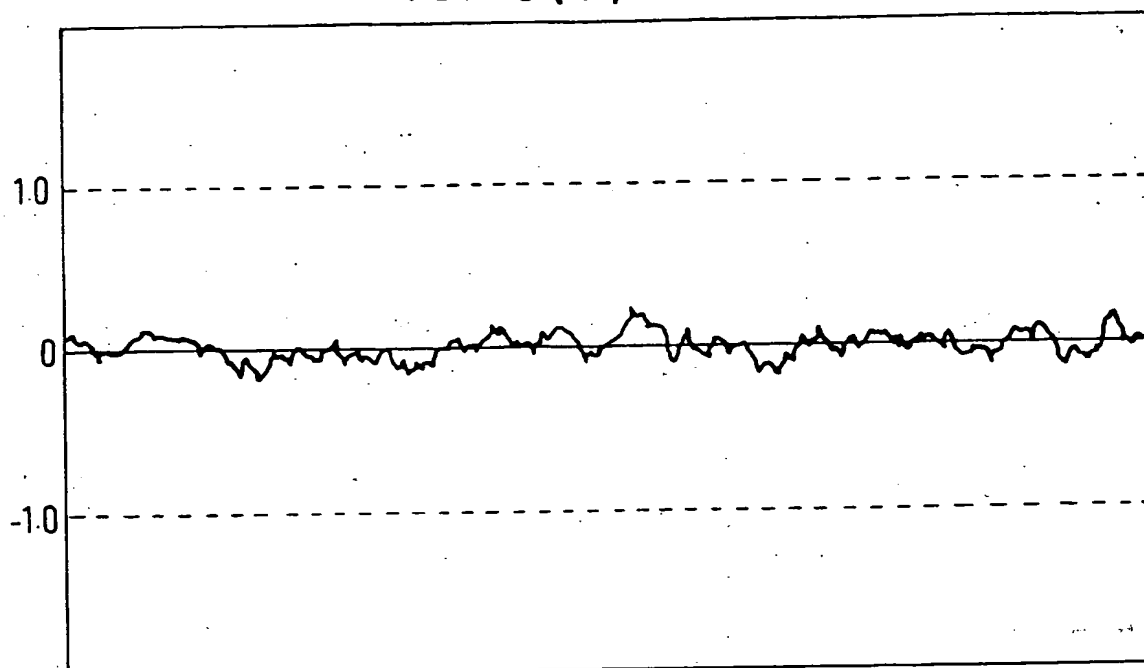


FIG. 9(b)

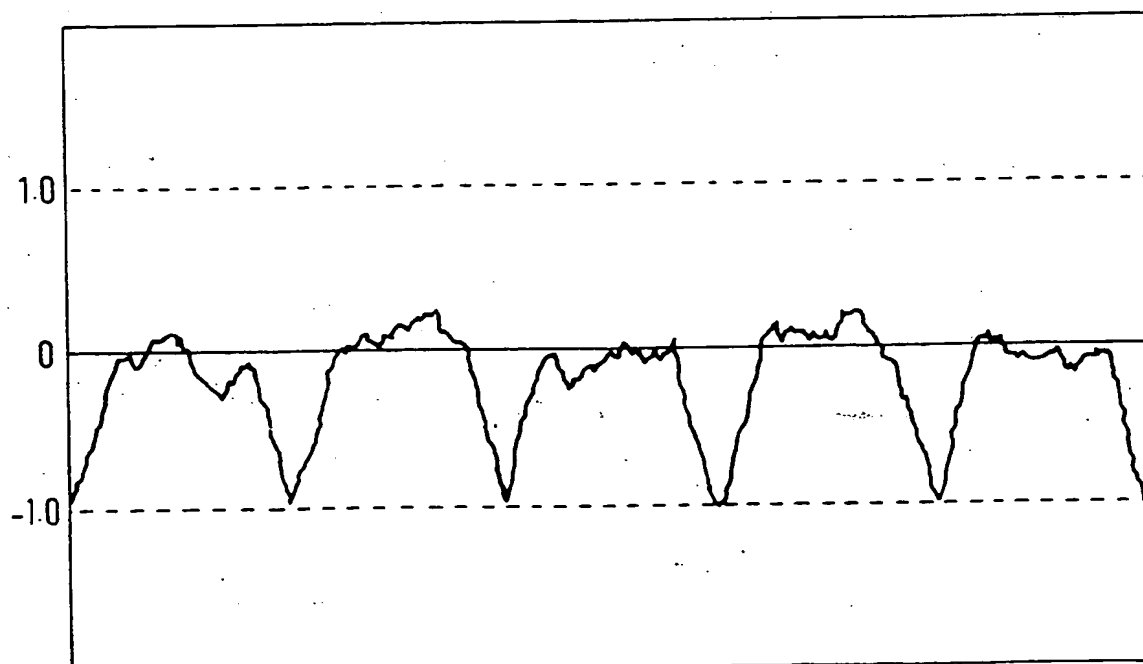


FIG. 10

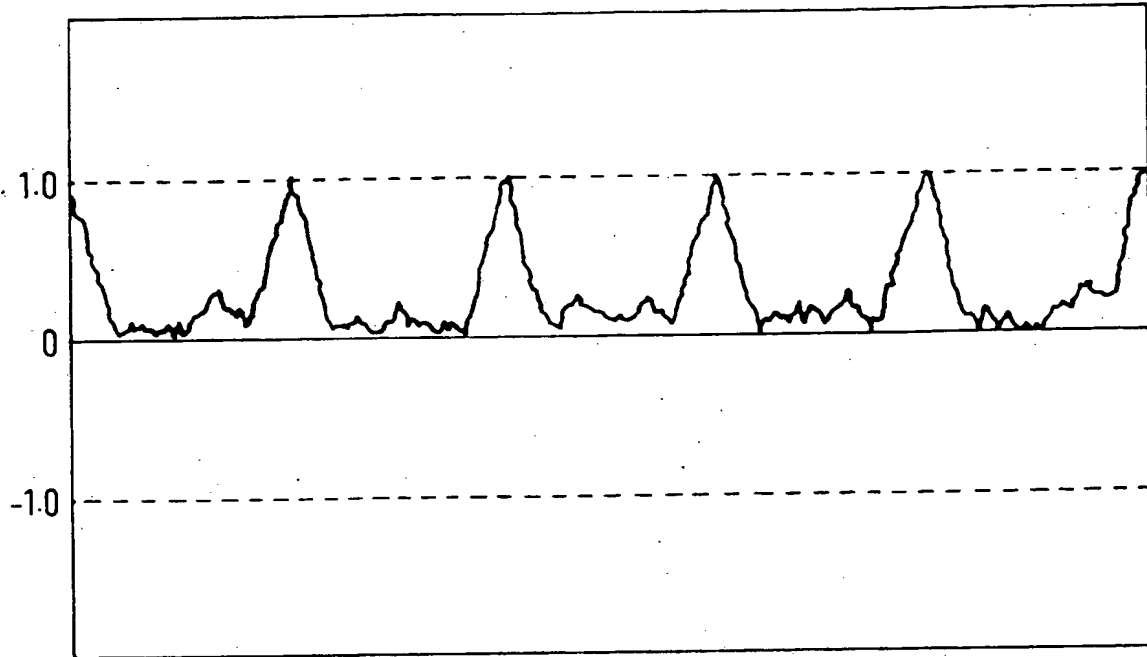


FIG. 15

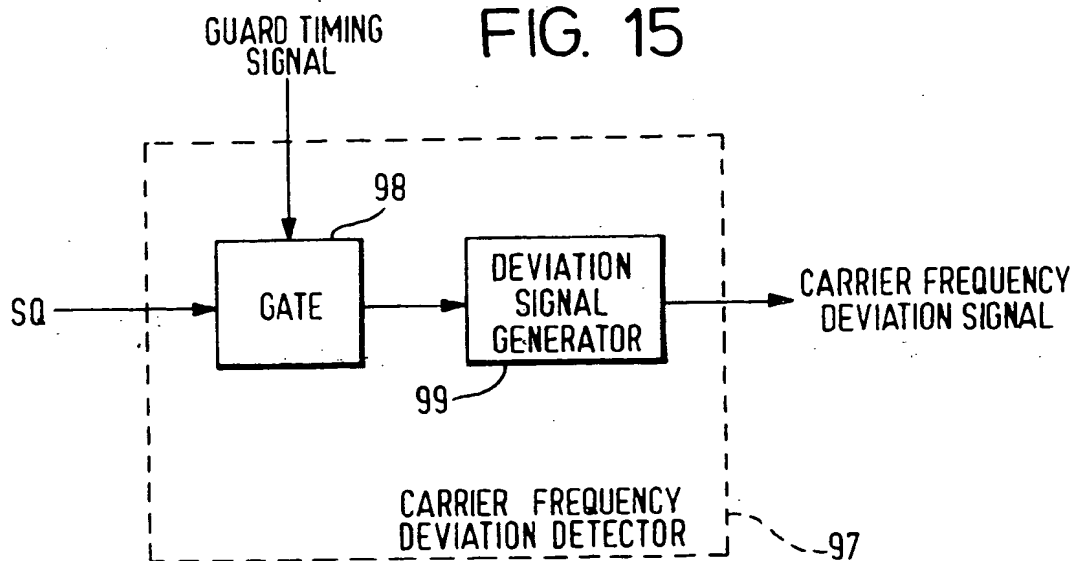


FIG. 11

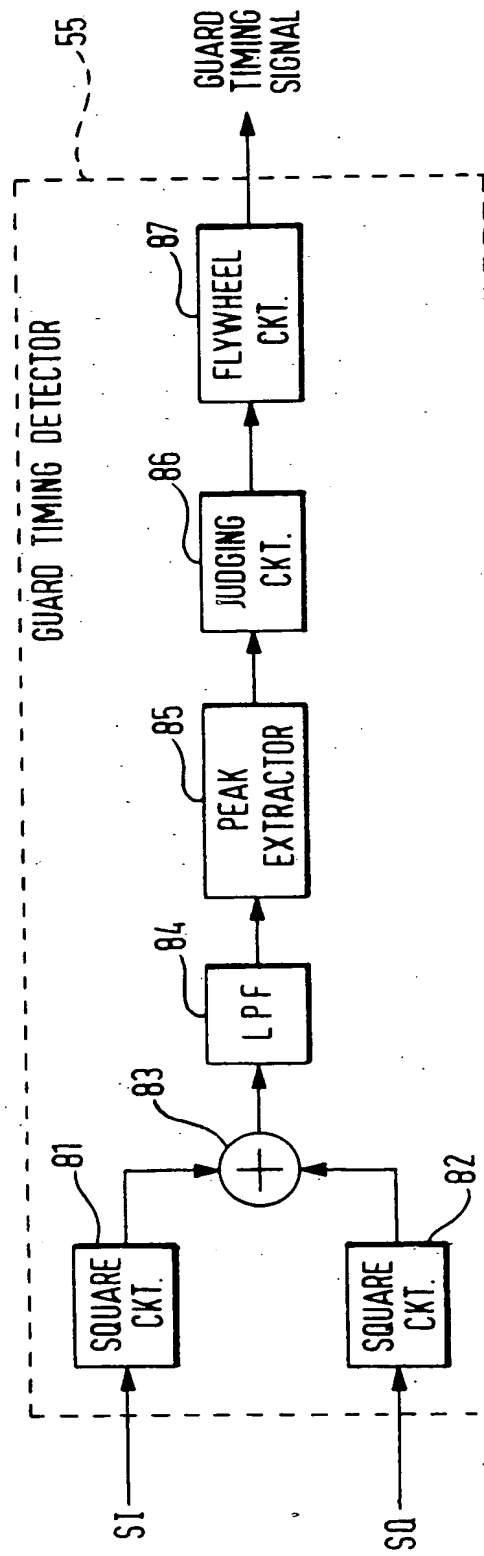


FIG. 12

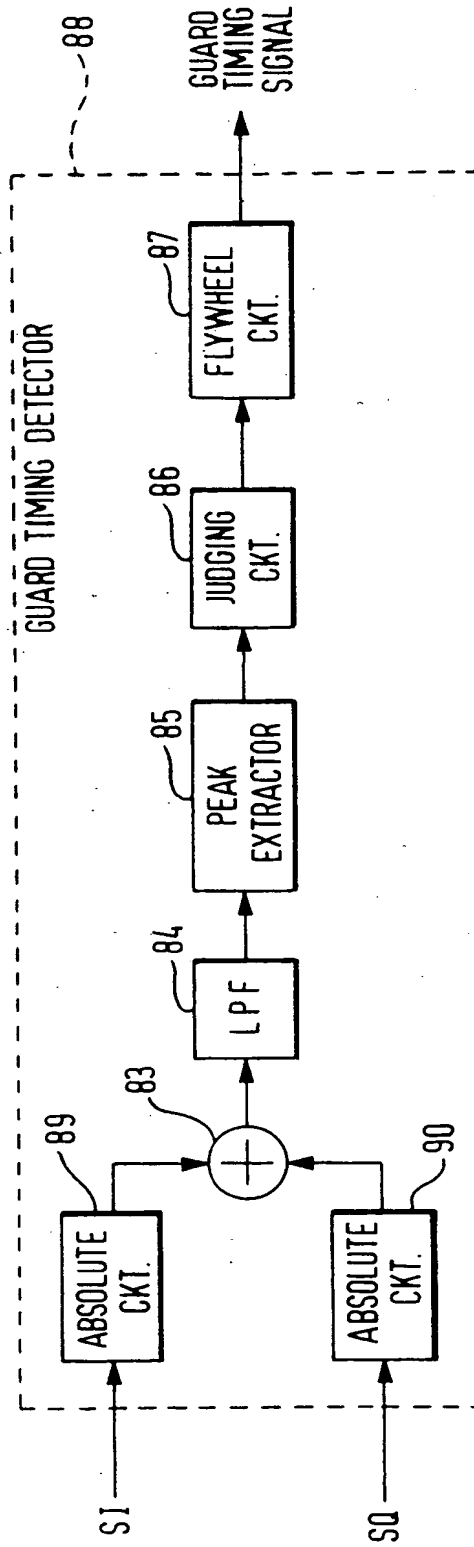
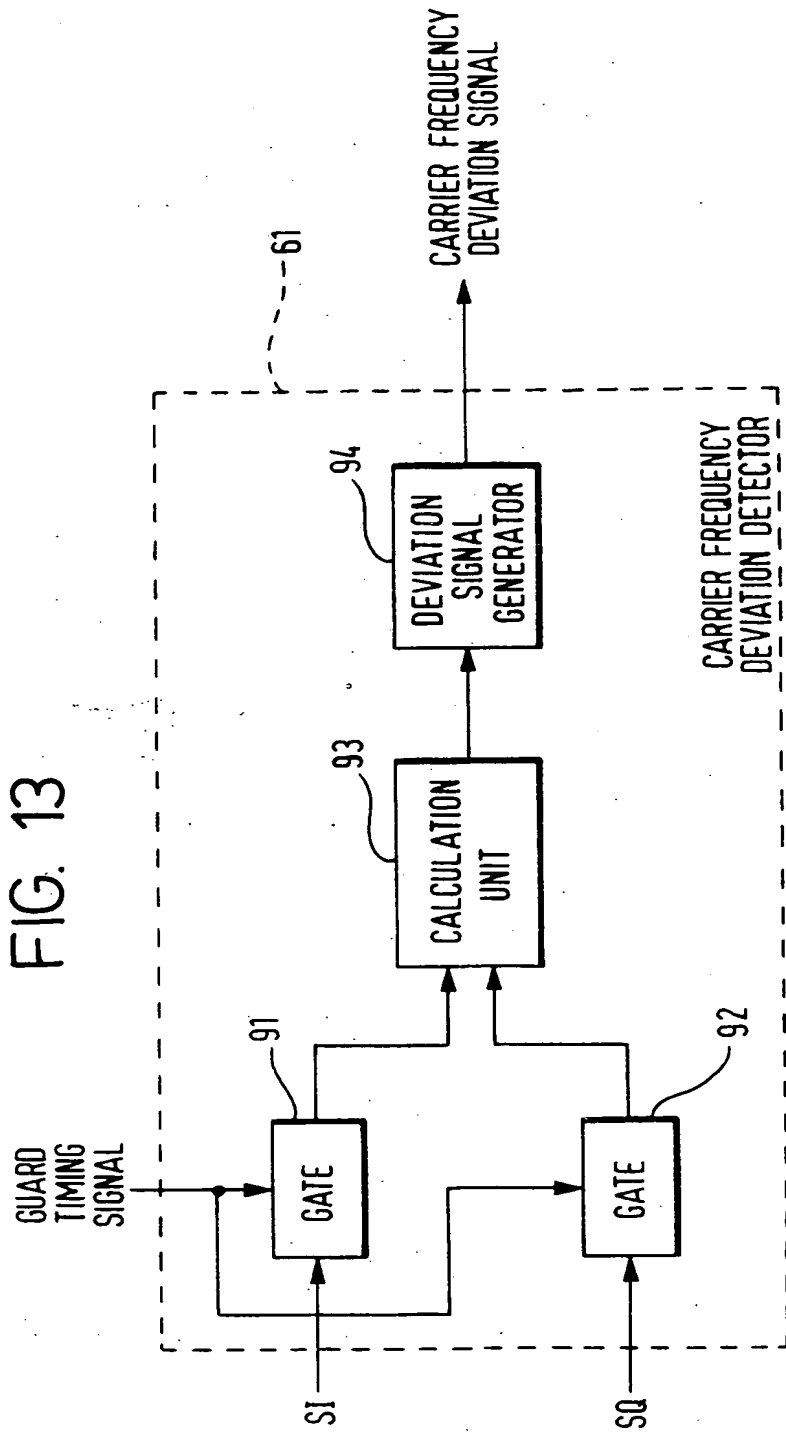
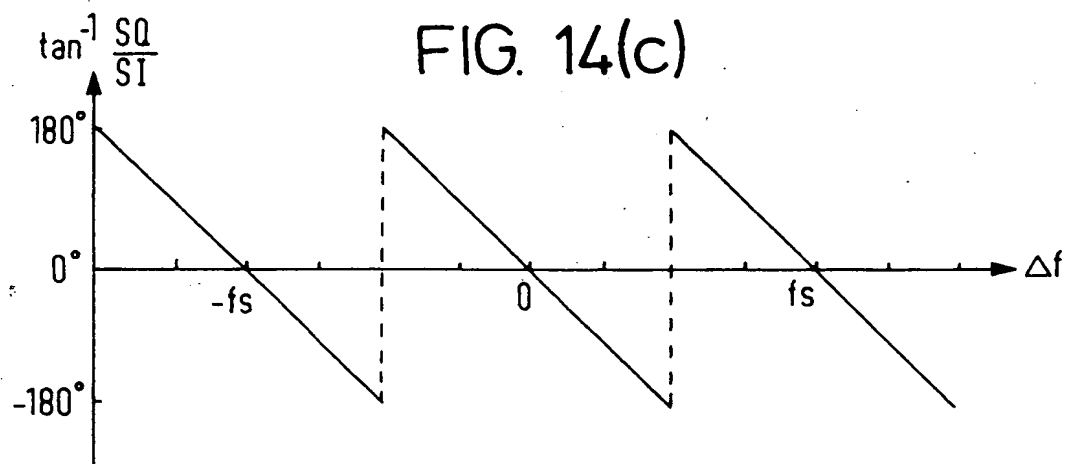
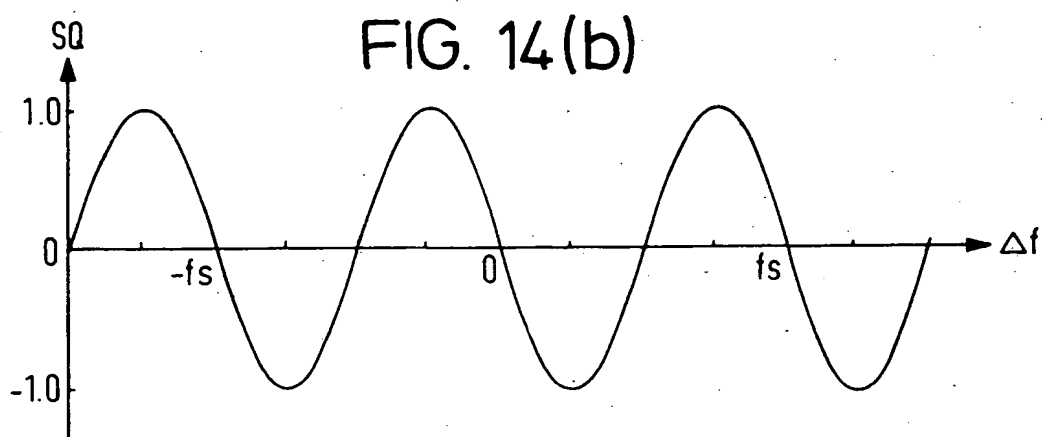
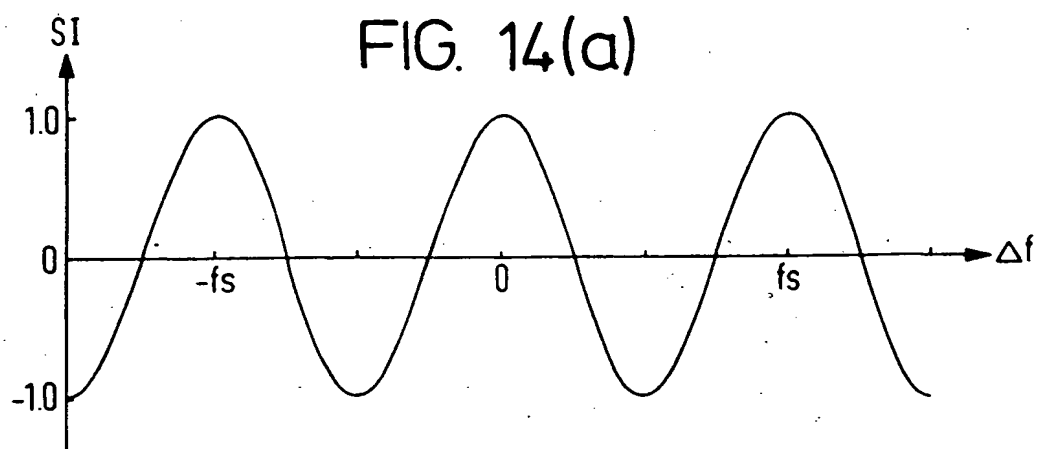


FIG. 13









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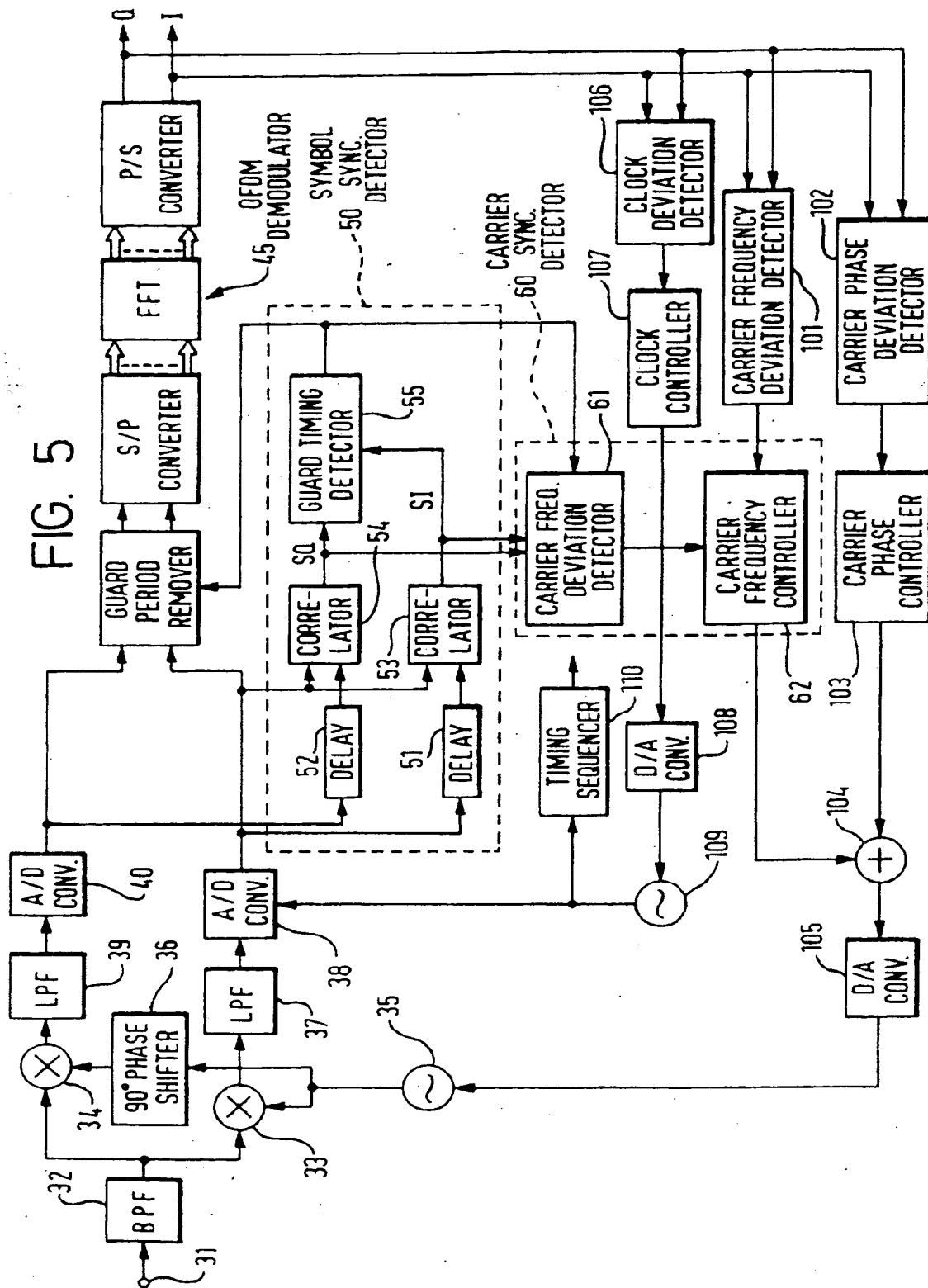
⑤④ **OFDM Synchronization demodulation circuit.**

⑤⑦ The invention provides an OFDM synchronization demodulation circuit which includes a receiving circuit for receiving an orthogonal modulated wave of an orthogonal frequency division multiplex (OFDM) modulated signal having an available symbol period and a guard period in waveform which coincides with a part of the available symbol period, an orthogonal axes demodulation circuit for demodulating an in-phase axis detection signal and an orthogonal axis detection signal through orthogonal detection for the OFDM modulated wave from the receiving circuit, a first delay circuit for delaying the in-phase axis detection signal by the available symbol period, a second delay circuit for delaying the orthogonal axis detection signal by the available symbol period, a correlation calculation circuit for calculating coefficients of the correlations of the in-phase axis detection signal and the orthogonal axis

detection signal from the orthogonal demodulation circuit with the output of the first or the second delay circuits, a guard timing detection circuit for detecting a timing of the guard period in the demodulation outputs from the orthogonal demodulation circuit, and an OFDM signal demodulation circuit for demodulating the OFDM modulated signal by extracting the available symbol period signal only from the demodulated output of the orthogonal demodulation circuit using the timing signal.

**EP 0 653 858 A3**

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European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 94 30 8433

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON COMMUNICATIONS (ICC), GENEVA, MAY 23 - 26, 1993, vol. 1 - 2 - 03, 23 May 1993 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 766-771, XP 000371188 FLAVIO DAFFARA ET AL 'MAXIMUM LIKELIHOOD FREQUENCY DETECTORS FOR ORTHOGONAL MULTICARRIER SYSTEMS' * abstract; figures 5,9 * * page 767, right column, paragraph 4 - page 768, right column *	1,4,5,8	H04L5/06
A	WO-A-92 10043 (THOMSON CSF) 11 June 1992 * abstract *	1,4,5,8	
A	EP-A-0 453 203 (TELEBIT CORP) 23 October 1991 * abstract; figure 2 *	1,4,5,8	
A	EP-A-0 365 431 (THOMSON CSF) 25 April 1990 * abstract *	1,4,5,8	<b>TECHNICAL FIELDS SEARCHED (Int.Cl.6)</b> H04L
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>29 August 1995</b>	Examiner <b>Scriven, P</b>
<b>CATEGORY OF CITED DOCUMENTS</b> X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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